IN THE SPECIFICATION:

Please amend the specification as follows:

Please amend the paragraph bridging pages 6 and 7, from line 15 on page 6 to line 2 on page 7, as follows:

If a voltage generation circuit which makes the potential of the source lines equal to the precharge potential of the bit lines in standby state, as mentioned above, is adopted, the voltage generation circuit is preferably constituted as follows: the voltage generation circuit discharges the source lines in response to an instruction to transition from standby state to active state. Further, the current supplying capability thereof is varied so that the discharge ~~discharg~~ rate will be enhanced stepwise. Fundamentally, the source lines only have to have capability to pull in currents passed through memory cells selected in active state. The foregoing is for preventing currents from concentratedly flowing from a large number of memory cells to such source lines at a time. Thus, the production of relatively large noise is prevented.

Please amend the paragraph bridging pages 20 and 21, from line 15 on page 20 to line 13 on page 21, as follows:

The microcomputer 1 has standby state and active state. "Active state" is a state in which the CPU 2 is capable of processing data in synchronization with the clock signal CK and the access operation of the ROM 3 and the RAM 4 is enabled by the CPU 2 and the like. After reset is released, the microcomputer 1 is brought into active state, though this is not an absolute requisite. Entrance into standby state is instructed by the standby signal STB, an external control signal, though this is not restricted. Alternatively, it is instructed by the CPU 2 setting a standby flag (not shown) on the system controller 9. "Standby state" is a state in which the operations of the CPU 2, the ROM 3, and the like are stopped. That is, it is a state in which the CPU 2 is incapable of processing data and the access operation of the ROM 3 and the like is disabled by the CPU 2. Standby state is also referred to as "wait state" or "low-power consumption state." More particularly, it is a state in which, for example, the clock generating operation of the CPG 8 is stepped; the operation of the CPU 2 is stopped (the contents of the internal registers are maintained); information stored in the RAM 4 is maintained; the operation of the peripheral circuit 6 is stopped; and the operation of the ROM 3 is stopped. The standby state of the microcomputer 1 (also referred to as "chip standby

state") is also a state in which the operation of the ROM 3 is stopped, that is, the standby state of the ROM 3.

Please amend the paragraph bridging pages 25 and 26, from line 20 on page 25 to line 2 on page 26, as follows:

The MOS transistors MP2 and MP3 [[NP3]] which receive the internal standby signals stb1 and stb2 at their gates charge the source lines to supply voltage VCC when the microcomputer 1 transitions to standby state. Thus, when the microcomputer 1 is in standby state, all the bit lines represented by BL1 and BL2 and all the source lines represented by SL and GSL are brought to supply voltage VCC. Thus, a potential difference is not produced between the source and drain of each memory cell MCi, and sub-threshold leakage does not occur there.

Please amend the paragraph bridging pages 33 and 34, from line 24 on page 33 to line 5 on page 34, as follows:

FIG. 16 illustrates another example of the microcomputer. The microcomputer 31 illustrated in the figure is a microcomputer for IC card (so-called IC card microcomputer), though ~~thought~~ this is not an absolute requisite. The microcomputer 31 illustrated in the figure is formed, on a semiconductor substrate or semiconductor chip, of single crystal silicon or the like, for example, by CMOS semiconductor integrated circuit manufacturing technology.